A 4 bits per cell 8Gb NROM Data-Storage Memory with Enhanced Write Performance

Ran Sahar¹, Avi Lavan¹, Eran Geyari¹, Amit Berman¹, Itzic Cohen¹, Ori Tirosh¹, Kobi Danon¹, Amichai Givant¹, Yoram Betser¹, Alexander Kushnarenko¹, Yaal Horesh¹, Boaz Eitan¹, Yair Sofer¹, Ron Eliyahu¹, Eduardo Maayan¹, Wang Pei Jen², Yan Feng², Lin Ching Yao², Kwon Yi Jin², Kwon Sung Woo², Cai En Jing², Yi Jing Jing², Kim Jong Oh², Yi Guan Jiun²

¹ Saifun Semiconductors Ltd. Israel,

² SMIC International Co. Ltd. China
Agenda

• The QUAD NROM Basics & Challenges
• General Architecture
• Multi Level Parallel Program & Verify
• Read & Sensing Method
• Constant Current Erase Technique
• Summary
• The QUAD NROM Basics & Challenges
  • General Architecture
  • Multi Level Parallel Program & Verify
  • Read & Sensing Method
  • Constant Current Erase Technique
  • Summary
The Quad NROM Basics

- Two storage areas per cell
- Each storage area is Multi-Level

- Two phase Program algorithm
- Error Detection + Moving Read algorithm

Four bits per cell

Reliability
The Write Performance Challenges

• Fast Programming & Narrow Vt distributions
  • Parallel Programming and Verify algorithm
  • Multiple Bit Line Voltage Programming
• Fast Erase with no over erase
  • Constant current Erase algorithm
• Fast and reliable Read

Page program speed   >4.5MB/s
Program Vt distribution  <350mV
• The QUAD NROM Basics & Challenges

• General Architecture

• Multi Level Parallel Program & Verify

• Read & Sensing Method

• Constant Current Erase Technique

• Summary
• The QUAD NROM Basics & Challenges
• General Architecture
• Multi Level Parallel Program & Verify
• Read & Sensing Method
• Constant Current Erase Technique
• Summary
The challenge for fast program
Many “bits” to be programmed
Different target Vt & different “bits” conditions
  Different target Vt – e.g. 01, 00, 10
  Different conditions – “other half cell” having one of 11, 01, 00, 10 target Vt
Dual BL Voltage Concept - Motivation

- Programming speed of one storage area depends on the state of the other storage area
- A “bit” with a programmed second bit will program faster than an erased second bit
Parallel Program Principles

• QUAD programming uses different BL voltages (VPPD) per level:
  • Level “01” is programmed via VPPD_{01_1}, VPPD_{01_2}
  • Level “00” is programmed via VPPD_{00_1}, VPPD_{00_2}
  • Level “10” is programmed via VPPD_{10_1}, VPPD_{10_2}

• All levels end programming at the same time
• Minimal number of pulses
Hex Bit Line Driver Circuit

Driver Sequence

Pre-charge
Gn_2
Gn_1
VDD SF_bias - Vt

LVL_MUX

VPPD01_1in
VPPD01_2in
VPPD00_1in
VPPD00_2in
VPPD10_1in
VPPD10_2in

PS_BLOCK

SF_bias

Drain_Charge_Pump

LVL_01
LVL_00
LVL_10
VPPD_1_2

Pre-charge
Gn_1
Gn_2

Parallel Program-Verify Principles

- All Program levels are verified simultaneously
- Based on the expected data, the correct Verify level is selected
• The QUAD NROM Basics & Challenges
• General Architecture
• Multi Level Parallel Program & Verify
• **Read & Sensing Method**
• Constant Current Erase Technique
• Summary
Sensing Method & Read

• Sensing Method:
  • Drain sensing – High Accuracy
  • VDD driven sensing – Low Power
  • All levels sensed at once – High Speed

• Read Challenges:
  • Process parameters variations
  • Virtual Ground array effects
  • Data pattern dependencies

  Read margin loss
Drain Driver Circuit – Basic Concept

- N-bias defines the current ($I_t$) of the drain driver
- P-bias defines the voltage ($V_{DR}$) of the drain driver
- The sensing current is: $I_{int} = I_t - I_{cell}$
  - $T1$ (NMOS) serves as a source follower, capable to supply all its pipe current (even if high) without drop penalty
Sense Amplifier with Offset Cancellation

Operation:

1. Offset cancellation period: $o_1$ & $in_1$ are shorted $\rightarrow$ Left plate of $C$ is at $DC_{Ref}$, $o_1$ & $in_1$ at inverter’s trip point

2. Initialization period: $SA_{IN}$ & $in$ are discharged to GND $\rightarrow$ $in_1$ follows by $C$ coupling to $V_{trip\_point} – DC_{Ref}$

3. NROM cell signal integration period: $SA_{IN}$ integrates from GND $\rightarrow$ Outputs ($o_1$ & $o_2$) will flip when $SA_{IN}$ crosses $DC_{Ref}$
The Virtual Ground Pipe Effect

I_{cell1} = I_{cell2}, I_{pipe1} > I_{pipe2} (Different neighbors state)

\[ I_{sense1} < I_{sense2} \]

- Pipe current should be minimized!
- Achieved by a Proper Physical order sequence
Read Order Principles

- Reading all bits in slice by 4 steps → Pre-defined Sequential order
- Stepping 2 cells at a time → Drain MBL is maintained (Power)
- Drain side is facing the isolation and maintained till end of the slice
- MBL’s change is followed by a pre-charge phase → Keeps Drain diffusion Bit Lines at same potential in sensing
- Discharge the slice at the end, before next read cycle → same initial conditions
• The QUAD NROM Basics & Challenges
• General Architecture
• Multi Level Parallel Program & Verify
• Read & Sensing Method
• Constant Current Erase Technique
• Summary
Accessing the Array for Erase

- The challenge for fast erase
- Many cells to be Erased → Too high current consumption
  - The Erase mechanism - TEHH band to band
  - Peak Erase current suppression is necessary for erase parallelism
Constant Current Erase - Motivation

- Erase current characteristics →
  Peak current at the beginning of the erase pulse

- Maximum bit counts are limited by the Peak current
- Average current is lower than the maximum allowed—inefficient!
Constant Current Erase - Technique

- Implement an erase pulse shape, that will enable the erasure of maximum bit count, within the limitation of the erase active maximum current
- Bit Line erase voltage will be ramped to the target voltage level
- Charge Pump current is continuously monitored and the voltage ramp rate adjusted, to prevent current from exceeding the specified limit

- Parameters for optimization: Bit count, target VPPD level, initial VPPD level
Constant current Erase - Product Results

Figure 1: VPPD target is increased according to algorithm, active current is following the VPPD increment, Charge pump is constant for each erase pulse phase.

Figure 2: VPPD rises only when Active current is lower than the maximum current allowed.
• The QUAD NROM Basics & Challenges
• General Architecture
• Multi Level Parallel Program & Verify
• Read & Sensing Method
• Constant Current Erase Technique

• Summary
8Gb Data Flash Features

- Technology: 90nm NROM technology
- Cell size: 0.036µm²/cell
- Die size: 155mm²
- Page Size: 4KB
- Power supply: 2.7V ÷ 3.6V
- Read cycle: 30ns
- Write cycle: 30ns
- Page program speed: >4.5MB/s
NROM Quad 90nm 8Gb Summary

- Fast & Accurate Programming
  - Two Phase Algorithm
  - Parallel Program & Verify
- Constant Current Erase

- Sequential Read for Pipe Effect Cancellation
  - Drain Sensing & Error Detection

Enhanced Write Performance

Reliability
For additional multimedia material: See http://www.isscc.org